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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,253	08/27/2003	Yuan-Jen Chao	4459-0149P	5216

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EXAMINER	
GETACHEW, ABIY	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
05/30/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/648,253	CHAO, YUAN-JEN	
	Examiner	Art Unit	
	ABIY GETACHEW	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-13,15,16 and 19-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-13,15,16 and 19-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4, 9-13, 15, 16 and 19-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Feldman (US 6,097,857).

Regarding claim 1, Fedman teaches a multi-chip integrated module (Fig. 5 and Fig.6), Comprising: a transparent substrate (Fig. 6, element 17'), which has a circuit layer formed on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter-connection (Fig. 6, elements 47) and a plurality of electrical pads (Fig. 6, elements 20'); at least two chips (Fig. 5, elements 13' and 15'), which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system; and a circuit substrate (Fig. 6, element 45), which attaches to the transparent substrate, and at least comprises a circuit layer (Fig. 6, element 40') of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate, wherein at least one gap (See Fig. 6 and Fig.7) is located between the chips (Fig. 5 element 46) and the circuit substrate (Fig. 6, element 45).

Regarding claim 2, as applied claim 1 above Fedman teaches, wherein the transparent substrate is glass substrate (Fig. 6 element 17').

Regarding claim 3, as applied claim 1above Feldman teaches that a plurality of bumps (Fig. 6, element 24') are formed on the electrical pads of the transparent substrate, respectively, for electrically connecting the electrical pads and the circuit layer of the circuit substrate(Fig. 6, element 45).

Regarding claim 4, as applied claim 1above Feldman teaches, Feldman teaches that a plurality of bumps are formed on a part of the circuit for electrical inter-connection (Fig. 6, elements 47) , and the chips electrically connect to the bumps by way of a flip-chip bonding (Fig. 6, elements 24').

Regarding claim 9, as applied claim 1 above Feldman teaches, a heat dissipation element (Fig. 5, element 45 and 11') is formed on the backside of at least one of the chips (Fig. 5 element 46).

Regarding claim 10, as applied claim 1 above Feldman teaches, that the circuit substrate is a printed circuit substrate (Fig. 6, element 45).

Regarding claim 11, as applied claim 1 above Feldman teaches a passive component (Fig. 6, element 25'), which is formed on the transparent substrate and electrically connects to the circuit for electrical inter-connection on the transparent substrate (Fig. 6, element 17').

Regarding claim 12, as applied claim 1 above Feldman teaches an active component (Fig. 6, element 13'), which is formed on the transparent substrate and

electrically connects to the circuit for electrical inter-connection on the transparent substrate.

Regarding claim 13, Feldman teaches a multi-chip integrated module, comprising: a transparent substrate (Fig. 6, element 17'), which has a circuit layer formed on one surface of the transparent substrate, wherein the circuit layer formed on the surface of the transparent substrate comprises a circuit for electrical inter- connection (Fig. 6, element 47), a plurality of bumps (Fig. 6, element 24') are formed on a part of the circuit for electrical inter-connection; a plurality of electrical pads (Fig. 6, elements 20') for electrical external connection and plurality of bumps (Fig. 6, element 24') formed on the electrical pads (Fig. 6, elements 20') respectively and at least two chips (Fig. 5, elements 13' and 15'), which electrically connect to the bumps of the circuit for electrical inter-connection by way of a flip-chip bonding, wherein the chips and the circuit for electrical inter-connection construct a circuit system, wherein the height of the first bumps are larger then the height of the chip (See figure 5 element 46).

Regarding claim 15, as applied claim 13 above Feldman teaches wherein the transparent substrate is glass substrate. (Fig. 6 element 17').

Regarding claim 16, as applied claim 13 or 14 above Feldman teaches, Feldman teaches the bumps are solder bumps (Fig. 6, element 24').

Regarding Claims 19 and 20 are rejected with the same logic as claims 11 and 12.

Regarding claim 21, Feldman teaches a multi-chip integrated module (Fig.5 and Fig.6), comprising: a transparent substrate (Fig. 6, element 17'), which has a circuit layer (Fig. 6, element 40') formed directly on one surface of the transparent substrate

(Fig. 6, element 17') , wherein the circuit layer (Fig. 6, element 40') formed on the surface of the transparent substrate (Fig. 6, element 17') comprises a circuit for electrical inter-connection and a plurality of electrical pads (Fig. 6, elements 20');
at least two chips (Fig. 5, elements 46), which are respectively mounted on the transparent substrate by way of a flip-chip bonding, wherein the chips (Fig. 5, elements 46) and the circuit for electrical inter-connection construct a circuit system; and
a circuit substrate, which attaches to the transparent substrate (Fig. 6, element 17'), and at least comprises a circuit layer of the circuit substrate, wherein the electrical pads of the transparent substrate electrically connect to the circuit layer of the circuit substrate, the circuit substrate (Fig. 6, element 45) has a hollow portion, and when the circuit substrate attaches to the transparent substrate, the chips are positioned in the hollow portion of the circuit substrate, wherein at least one Rap (See Fig. 6 and Fig.7 i.e. Rap define as crack or gap) is located between the chips (Fig. 5, elements 13' and 15') and the circuit substrate (Fig. 6, element 45).

Regarding claim 22, as applied claim 21 above Fedman teaches, wherein the transparent substrate is glass substrate (Fig. 6 element 17').

Regarding claim 23, as applied claim 21above Feldman teaches that a plurality of first bumps (Fig. 6, element 24') are formed on the electrical pads (Fig. 6, elements 20') of the transparent substrate (Fig. 6, element 17'), respectively, for electrically connecting the electrical pads and the circuit layer (Fig. 6, element 40') of the circuit substrate (Fig. 6, element 45).

Regarding claim 24, as applied claim 21above Feldman teaches, wherein a plurality

of second bumps (Fig 6 element 47) are formed on a part of the circuit for electrical inter-connection, and the chips electrically connect to the second bumps (Fig 6 element 47) by way of a flip-chip bonding (Fig. 6, elements 24').

Regarding claim 25, as applied claim 21above Feldman teaches a heat dissipation element (Fig. 5, element 45 and 11') is formed on the backside of at least one of the chips.

Regarding claim 26, as applied claim 21 above Feldman teaches that the circuit substrate is a printed circuit substrate (Fig. 6, element 45).

Regarding claim 27, as applied claim 1 above Feldman teaches wherein the chips (Fig. 5, elements 13' and 15') and the circuit substrate are located at the same side of the transparent substrate (Fig. 6, element 17').

Regarding claim 28, as applied claim 2 above Feldman teaches wherein the pitches [Column 1 paragraph 5 lines 65-66 and column 2 paragraph 1 lines 1-2] of the circuit for electrical inter-connection (Fig 6 element 47) are below 100 micrometer.

Regarding claim 29, as applied claim 13 above Feldman teaches, wherein the chips (Fig. 5, elements 46) and the first bumps are located at the same side of the transparent substrate (Fig. 6, element 17') .

Regarding claim 30, as applied claim 15 above Feldman teaches wherein the pitches of the circuit for electrical inter-connection are below 100 micrometer. [Column 1 paragraph 5 lines 65-66 and column 2 paragraph 1 lines 1-2]

Regarding claim 31, as applied claim 21 above Feldman teaches wherein the chips and the circuit substrate are located at the same side of the transparent substrate (Fig.

6, element 17').

Regarding claim 32, as applied claim 22 above Feldman teaches wherein the pitches of the circuit for electrical inter-connection are below 100 micrometer. [Column 1 paragraph 3 lines 34-45 i.e. a multichip module capable of providing such a large number of interconnections per chip is desired]

Response to Arguments

2. Applicant's arguments filed on 02/05/2008 have been fully considered but they are not persuasive.

First Applicants argue "The Feldman reference does not teach the pitches of the interconnection lines being below 100 micrometer"

Examiner Disagree: because Feldman teaches that the chips may arranged so that optical transmitters and detectors are on a common circuit plane, different circuit planes, or a mixture of both. Applicant's attention respectfully directed to [Column 1 paragraph 5 lines 65-66 and column 2 paragraph 1 lines 1-2]

Second, Applicants argue "claim 21 is a third independent claim which also describes the two chips being mounted on the transparent substrate, which is not seen in the reference"

Examiner Disagree: because Feldman teaches that pluralities of chips are mounted on a substrate in an inverted position so that the electrical connection pads are exposed on the upper surface of the chip. Applicant's attention respectfully directed to [Column 1 paragraph 5 lines 52-58]

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABIY GETACHEW whose telephone number is (571)272-6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DEAN REICHARD can be reached on (571)272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean A. Reichard/
Supervisory Patent Examiner, Art Unit 2841

Abiy Getachew
Examiner
Art Unit 2841

A.G.
May 23, 2008